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FORM PTO-1390 (REV 10-95) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY DOCKET NUMBER: 15675P372

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 09/936487

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR00/00559	March 7, 2000	March 8, 1999

TITLE OF INVENTION: METHOD FOR TESTING INTEGRATED CIRCUITS WITH MEMORY ELEMENT

APPLICANT(S) FOR DO/EO/US: Dominique Barthel

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b)) and PCT articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A subsequent specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:

priority request; formal drawings transmittral; preliminary examination report w/amended pages; preliminary examination report; english translation of the amended pages; copy of forms pct/ib 301, 304; pct filing receipt; complete copy of application w/amended pages (23 pages)

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/936487	PCT/FR00/00559	15675P372

17. ☒ The following fees are submitted:

	CALCULATIONS FOR PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):	
Neither international preliminary examination fee (37 CFR 1.482 nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by EPO or JPO **$1000.00**	
International preliminary examination fee (37CFR1.482)not paid to USPTO but International Search Report prepared by the EPO or JPO.... **$860.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee paid to USPTO (37 CFR 1.445(a)(2)) **$700.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	27 - 20 =	~~7~~	X $18.00	$ 126.00~~130~~
Independent claims	~~3~~ - 3 =	0	X $78.00	$ 0.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$ 270.00
TOTAL OF ABOVE CALCULATIONS =				$ 1256.00~~1130.00~~
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).				$
SUBTOTAL =				$ 1256.00~~1130.00~~
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$
TOTAL NATIONAL FEE =				$ 1256.00~~1130.00~~
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$
TOTAL FEES ENCLOSED =				$ 1256.00~~1130.00~~
			$ Amount to be: refunded	$
			charged	$

a. ☒ A check in the amount of $ 1130.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 022666. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Blvd. 7th Floor
Los Angeles, CA 90025-1026

SIGNATURE

Eric S. Hyman
NAME

30,139
REGISTRATION NUMBER

Atty. Docket No.: 1567.933
Express Mail #: EL651820244US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the application of:)
)
Dominique Barthel)
)
For: METHOD FOR TESTING INTEGRATED CIRCUITS)
WITH MEMORY ELEMENT)

PRELIMINARY AMENDMENT

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified application, Applicant requests entry of the following amendment:

IN THE SPECIFICATION

At page 4, please delete the specification beginning at line 23 and ending on page 5, line 30 through the words "boundary scan claim" and replace with the following:

ESH:kla

accessible from outside the board, via one and the same path from a specific terminal of the board, the transfer of the data sensed or to be imposed taking place in series in this path.

Through such arrangements, the Boundary Scan also permits the testing of the interconnections between the integrated circuits on a board. In this case, the test vector is loaded serially into the Boundary Scan path, then sent to the interconnections to be tested via output buffers of the components. The results are sampled in the Boundary Scan, via the inputs of the components, then output serially to the tester.

In an "internal test" mode, adapted for testing the components themselves, a test vector is loaded in

series in the Boundary Scan path and then applied to the internal logic of the integrated circuit. The result is sampled in the Boundary Scan path, then read serially by the tester.

This second test process has drawbacks: it is especially lengthy to implement, particularly in the internal mode where the components of the board are tested. Moreover, this test process turns out to be especially unsuitable for the testing of integrated circuits before they are mounted, in particular for testing integrated circuits which comprise memory elements.

US 5 850 513 also discloses a system allowing the checking of operational data of a circuit, including a maintenance subsystem, a flash memory, a controller, a processing unit, a main memory module, a data path network, means forming a dual bus, programmable logic control means, an auxiliary data transfer nozzle, and a series of input/output modules.

Together, these components process blocks of data of microcodes. The elements such as associated in this document, do not allow testing of the integrated circuit without multiple connections. This document does not therefore afford a satisfactory solution to the particularly lengthy implementation of customary testing processes.

The aim of the invention is to resolve these various drawbacks, by proposing a process for testing integrated circuits not requiring the connection of all the inputs/outputs of this circuit to a tester and making it possible to test an extended area, or even the entire circuit, it being possible moreover for this process to be carried out much faster than the known test processes.

Stated otherwise, the invention proposes to improve the coverage of an integrated circuit fabrication test as compared with the known full-scan ATPG method, without increasing the number of channels of the tester.

These aims are achieved according to the invention by virtue of a process for testing an integrated circuit comprising memory points and a Boundary Scan chain

REMARKS

Entry of the foregoing amendments is requested which correspond to amended sheets in the international application.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 9/10/01 By: ______________________

Eric S. Hyman, Reg. No. 30,139

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ESH:kla

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No. :

U.S. National Serial No. :

Filed :

PCT International Application No. : PCT/FR00/00559

VERIFICATION OF A TRANSLATION

I, Susan POTTS BA ACIS

Director to RWS Group plc, of Europa House, Marsham Way, Gerrards Cross, Buckinghamshire, England declare:

That the translator responsible for the attached translation is knowledgeable in the French language in which the below identified international application was filed, and that, to the best of RWS Group plc knowledge and belief, the English translation of the international application No. PCT/FR00/00559 is a true and complete translation of the above identified international application as filed.

I hereby declare that all the statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application issued thereon.

Date: August 17, 2001

Signature of Director :

For and on behalf of RWS Group plc

Post Office Address : Europa House, Marsham Way,
Gerrards Cross, Buckinghamshire,
England.

Process for testing integrated circuits with access to memory points of the circuit

The present invention relates to processes and devices for testing integrated circuits as well as the integrated circuits furnished with means permitting the carrying out of effective tests.

Two main processes for testing complex integrated logic circuits are known.

A first process, called the "full scan path automatic test pattern vector generation process" or "full scan ATPG" process is commonly used to test the fabrication of chips.

This process consists in injecting known signals onto pins of the integrated circuit and in tapping off the values obtained from the output pins, so as to compare them with expected values.

This process uses a tester whose channels are linked to the input/output pins of the integrated circuit. In order to implement this process correctly, one requires a tester having a number of channels equal to the number of input/output pins of the circuit.

With this process, one can test in particular a combinatorial logic function. Knowing the combinatorics, one can automatically generate the logic vectors which make it possible to verify in a quasi-exhaustive manner the correct implementation of the combinatorics.

However, when the function of the integrated circuit comprises memory elements, one cannot in general generate the test vectors. In certain rare cases where these vectors can be generated despite the presence of memory points, the number of test vectors is very high,

so that a very long test sequence must be implemented, this being difficult to store in memory, difficult to manipulate, and requiring a great deal of on-tester time.

To avoid this drawback in the case of integrated circuits having memory points, one can set in place in the circuit an access path to the memory points which makes it possible to read and write from/to all these memory points, in such a way that the function of the integrated circuit is reduced, by controlling the memory points, to a combinatorial function which can be tested.

Customarily, the memory points are placed in series on the access path, this access path being reserved for the test. This path is called the "full scan path". This access path adds a few inputs/outputs to the circuit.

This first process comprises a major drawback.

It necessitates a physical access, consisting of a channel of the tester, for each input/output of the integrated circuit. However, nowadays, the number of inputs/outputs of integrated logic circuits commonly exceeds several hundred, and will soon reach a thousand, and present-day testers can in practice only be made with a few hundred channels. Present-day testers are therefore becoming unsuitable for the integrated circuits to be tested.

More generally, the higher the number of channels of the testers, the more expensive the latter are.

This drawback is especially acute in the case of large-size circuits, which are most liable to exhibit operating faults. For such circuits, the test is carried out directly on a silicon slice, before lengthy

and expensive mounting of the circuit in a package, which could turn out to be fruitless since the circuit might be defective. Such an on-slice test is carried out with the aid of a plugboard, whose cost and complexity of construction increase more quickly than the number of plugs, especially by reason of a plug coplanarity constraint.

For these reasons, this ATPG method is implemented by linking only some of the input/output pins to the tester. Certain inputs/outputs therefore remain untested, to the detriment of the quality of the fabrication test, and areas of the circuit remain untested.

Thus, represented in figure 3 is a circuit tested with this known process, on which are indicated, by the reference 10, the unconnected leads, and on which the untested areas have been hatched.

A second process for testing integrated circuits is known, which allows the checking and observation of logic levels on the inputs/outputs of a circuit, even when the interconnections of the package are not physically accessible. This process is used in particular in the case of a surface-mounted ball grid package (BGA package), or else in the case of a multilayer printed circuit.

This second type of test, called the "JTAG Boundary Scan", and defined by the "Joint Test Action Group", IEEE standard 1149.1, relates essentially to the testing of printed boards and of the soldering of integrated circuits onto these boards. This IEEE standard 1149.1 makes provision for an access path to the inputs/outputs which is able to substitute for a direct physical connection to the inputs/outputs.

This second type of test is implemented by adding logic specific to this test into the integrated circuit and into the printed board which carries it, this logic making it possible, under the control of a handler called the TAP controller ("Test Access Port controller"), to sense the logic level present on an input, and/or to impose the logic level on an output of the integrated circuit. In normal mode, this logic is transparent, both to the inputs and to the outputs.

Thus, the integrated circuits of a board are furnished with an access path having the form of a loop and linking in series the set of inputs/outputs of the relevant circuit, and the loops of each of the integrated circuits are linked in series.

The Boundary Scan chain therefore runs around the component into which it is integrated, and also runs around the board receiving the components. A general Boundary Scan chain links the Boundary Scan chains of each component in series, so that each input/output pad of each component as well as each track of the board is accessible from outside the board, via one and the same path from a specific terminal of the board, the transfer of the data sensed or to be imposed taking place in series in this path.

Through such arrangements, the Boundary Scan also permits the testing of the interconnections between the integrated circuits on a board. In this case, the test vector is loaded serially into the Boundary Scan path, then sent to the interconnections to be tested via output buffers of the components. The results are sampled in the Boundary scan, via the inputs of the components, then output serially to the tester.

In an "internal test" mode, adapted for testing the components themselves, a test vector is loaded in series in the Boundary Scan path and then applied to

the internal logic of the integrated circuit. The result is sampled in the Boundary Scan Path, then read serially by the tester.

This second test process has drawbacks: it is especially lengthy to implement, particularly in the internal mode where the components of the board are tested. Moreover, this test process turns out to be especially unsuitable for the testing of integrated circuits before they are mounted, in particular for testing integrated circuits which comprise memory elements.

The aim of the invention is to resolve these various drawbacks, by proposing a process for testing integrated circuits not requiring the connection of all the inputs/outputs of this circuit to a tester and making it possible to test an extended area, or even the entire circuit, it being possible moreover for this process to be carried out much faster than the known test processes.

Stated otherwise, the invention proposes to improve the coverage of an integrated circuit fabrication test as compared with the known full-scan ATPG method, without increasing the number of channels of the tester.

These aims are achieved according to the invention by virtue of a process for testing an integrated circuit comprising memory points and a Boundary Scan chain, in which one writes and/or reads to and/or from the memory points by way of an access path to the memory points from an outside terminal of the circuit, characterized in that the Boundary Scan chain is activated so as to impose and/or observe logic levels on the inputs/outputs of the integrated circuit.

Other characteristics, aims and advantages of the invention will become apparent on reading the detailed

description which follows, with reference to the appended figures in which:

- figure 1 diagrammatically represents a purely combinatorial integrated circuit in accordance with the state of the art;

- figure 2 represents an integrated circuit comprising combinatorial functions and memory elements in accordance with the state of the art;

- figure 3 represents the same circuit as in figure 2, wherein hatched areas indicate areas not tested when employing an ATPG process of the state of the art;

- figure 4 represents an integrated circuit furnished with a Boundary Scan chain whose inputs and outputs have been represented in detail, in accordance with the state of the art;

- figure 5 represents an integrated circuit according to the invention, of which an access path to memory elements has been concatenated with a Boundary Scan path;

- figure 6 represents an integrated circuit according to the invention, in accordance with that of figure 5, and whose means of connection between the access path to the memory elements and the Boundary Scan path have been represented.

Represented on the integrated circuit of figure 4 are three main parts: two Boundary Scan input/output modules 20 and 30, and between these two modules, a part 40 forming the core of the integrated circuit.

The two modules 20 and 30 represented here are identical to one another. Each of the two modules 20 and 30 is placed in parallel with a direct link between

a connection pin and the core 40 of the chip.

Only the module 20 will be described, the module 30 comprising the same elements as the module 20.

The module 20 has two ends, each formed by a multiplexer 22, 24. On a link 23, a first 22 of these two multiplexers receives a control signal called "signal shift", which configures the cell as "shift" or as "load".

In the case of the cell 20 represented on the left in figure 4, the multiplexer 22 is able to receive a pin signal on its first input 21, this being for example a signal received from another chip of the board.

On a second input 23 of the multiplexer 22, the latter receives an input signal SI, carrying data transferred into the Boundary Scan chain and which data is intended to be loaded by the cell 20 if the latter is in "shift" mode.

Between the two multiplexers 21 and 24, the cell has two registers 25 and 26, one of which is a shift register 25 which delivers an output signal SO intended to be conveyed in the Boundary Scan to other input/output cells (not represented) of the chip 40, or else to other chips.

The shift register 25 also receives a clock signal denoted ck and the other register 26 receives a signal upd for updating the output latches of the cell 20, that is to say of memories of the cell 20 which are able to form a chosen logic level of this input or of this output of the integrated circuit, when this cell 20 is activated.

The shift register 25 also delivers a signal SO which contains, for certain cells, information captured on

this cell and/or representative of data recorded in the cell 20, and possibly intended to be analyzed so as to interpret the test.

SI is therefore the serial data input, SO the serial data output.

The multiplexer 24 situated at the other end of the cell 20, that is to say between the cell 20 and the core 40 of the chip, receives a "mode" signal able to control the cell 20 so that the signal transmitted by the cell 20 to the core of the chip 40 is not the signal received on the pin 21 but the signal consisting of the content of the latches of the cell 20.

The signals SI and SO are conveyed through the integrated circuit, from input/output cell to input/output cell over the entire Boundary scan loop linking these inputs/outputs in series.

In a known manner, such an integrated circuit comprises a TAP controller, not represented, whose role is to generate the control signals SHIFT, UPD, CK and MODE for the Boundary Scan chain of the integrated circuit.

When testing a board, the TAP controller itself receives control signals flowing through the Boundary scan path of the board. The instructions relating to logic levels to be imposed on certain cells of its integrated circuit are transmitted to the TAP controller of the circuit by these control signals. Conversely, logic levels captured on certain cells are also transmitted in the Boundary Scan path by the TAP controller.

The integrated circuit according to the invention, which is represented in figure 5, comprises a set of pins 100 each associated with an input/output cell 110. The cells 110 are coupled in series by a Boundary Scan

peripheral path 120, represented as a double dashed line. This peripheral path 120 therefore forms a loop 110 which runs around the perimeter of the circuit from input/output cell 110 to input/output cell 110.

This integrated circuit comprises combinatorial functions 130 and memory elements 140. The memory elements 140 are interlinked in series by a path 150 which makes it possible to access these memories from an outside pin 108. This path 150 makes it possible to control, during a test, the memories 140 directly from outside the circuit.

Among the pins 110, certain pins referenced 103 are linked to the channels of a tester (not represented) and other pins referenced 105 are not connected to the tester. The connected pins 103 are prolonged in figure 5 by a thick line, whereas the unconnected pins 105 merely have a short thin line.

In accordance with the invention, the testing of this integrated circuit is carried out by acting from outside on the memories 140, while activating the Boundary Scan path 120.

The path 150 is used either to place the memories 140 in a predetermined state, or else to capture their state in the course of the test. Simultaneously, the Boundary Scan path 120 is used to impose the predetermined logic levels on certain unconnected inputs/outputs 105 or to capture logic levels to be observed.

Thus, the memories 140 are acted on by way of the path 150 and the unconnected cells 105 are acted on by way of the Boundary Scan path 120.

In this mode of implementation of the invention, chosen signals are injected into the connected pins 103

directly through the channels of the tester.

The Boundary Scan path 120 being connected to the tester, the tester dispatches into this path a signal chosen specifically to activate certain of the other cells 105 which are not connected and to impose a predetermined logic level on them.

By using both the Boundary Scan path 120 and a direct connection of the pins 103, the tester has access to all the pins 100 of the integrated circuit. Any desired test vector can therefore be applied to a set of pins which encompasses connected pins 103 and unconnected pins 105.

Predetermined levels are applied to groups of input/output pins 100 by combining an action by direct connection on certain pins with an indirect action on the inputs/outputs by way of the Boundary Scan 120.

The invention also envisages that no pin be acted on directly and that the logic levels of the inputs/outputs not be imposed or read other than by way of the Boundary Scan, whilst acting directly on the memory elements 140 of the circuit through one or more direct accesses to these memories 140.

In the case of a circuit with fifteen memory elements for example, it is possible to adopt fifteen paths for direct access to each of the memories, the Boundary Scan forming a sixteenth control path for elements of the circuit. Of course, it is also possible to place fifteen memory elements in series on one and the same path as in the case of figure 5.

In the exemplary embodiment of figure 5, the access path 150 to the memory elements 140 is concatenated with the Boundary Scan path 120 so that these two paths form one and the same chain on which both the memory

elements 140 and also the input/output cells 110 are placed in series.

Thus, one acts on the memory points 140 and on the input/output cells 110 with the sole connection 108 outside the circuit, by injecting the serial data into this chain.

Represented in figure 6 is a setup adapted to such concatenation of the Boundary Scan chain 120 and of the chain 150 for direct access to the memories 140. This preferred setup exhibits the advantage of leaving the Boundary Scan path 120 available to the TAP controller when not implementing the test process according to the invention and of making it possible to activate the Boundary Scan path 120 during a test of the integrated circuit carried out in accordance with the invention.

To do this, the chain 150 for access to the memories 140 is linked to the Boundary Scan chain 120 by way of at least one multiplexer controlled by a mode signal ATPG-mode, injected from the pin 108.

In a conventional manner, the Boundary Scan chain 120 comprises six links. In figure 6, the Boundary Scan path 120 has been depicted diagrammatically by a simple rectangle furnished with six connections corresponding to these links.

Likewise, the assembly formed of the access path 150 with its memory elements 140 has been represented by a simple rectangle referenced 150.

Represented in detail is the junction between the part of the Boundary Scan chain comprising the cells 110 in series, the TAP controller 200 and the access path 140 which here is also called the full-scan ATPG path by reference to the prior art.

This splice is situated downstream of the TAP controller 200 on the Boundary Scan chain and downstream of the memory points 140 on the access path 150.

In this setup, the pin 108 forms the outside end of a set of four links flowing parallel to one another on the path 150 up to this junction.

These four links are:

- an ATPG-si link able to transmit an information carrier signal to the memory elements 140 and to the cells 110, controlling states of certain memories 140 or logic levels of certain inputs/outputs 110 which are able to recognize the signals which are specifically intended for them. This ATPG-si channel carries between the pin 108 and its junction with the Boundary Scan chain the memory elements 140 arranged in series;

- an ATPG-se link able to transmit to the Boundary Scan a "shift" or "load" configuring signal SE for the chosen cells of the Boundary Scan;

- a CLOCK link able to transport a clock signal CK to the various elements of the Boundary Scan, and;

- an ATPG-mode link able to convey a control signal MODE indicating whether the Boundary Scan 120 is to be linked to the controller 200 or else to the chain for access to the memories 150. In the latter case, the Boundary Scan chain 120 is linked in series to the ATPG chain 150.

The ATPG-mode link is linked to five multiplexers (or equivalent functions), each time constituting a control channel thereof.

A first multiplexer 210 receives on a first input the

signal SI conveyed on the ATPG-Si link and receives on a second input an input signal SI originating from the TAP controller 200.

On its two inputs a second multiplexer 220 respectively receives the clock signal CK coming from the pin 108 and another clock signal CK coming from the controller 200.

On its inputs a third multiplexer 230 respectively receives the signal SE originating from the pin 108 and the signal SHIFT coming from the controller 200.

On its two inputs a fourth multiplexer 240 respectively receives the mode signal originating from the controller 200 and a constant activation signal denoted "1".

On its two inputs a fifth multiplexer 250 respectively receives the updating signal UPD originating from the controller 200 and a constant activation signal denoted "1".

When the mode signal which is injected into the pin 108 on the ATPG-mode link is at 0, the SI, MODE, Shift, CK and UPD links of the Boundary Scan 120 are linked, as in an ordinary circuit, to the controller 200.

Stated otherwise, when no activated test mode signal is transmitted in the pin 108, the Boundary Scan 120 is linked to its control device 200 contrived for carrying out a standard Boundary Scan test.

On the other hand, when a test activation signal is transmitted on the ATPG-mode channel of the pin 108, the SI, CK, SHIFT channels of the Boundary Scan 120 are linked respectively to the signals SI, CK, SE applied respectively to the ATPG-Si, Clock and ATPG-Se links of the pin 108, whilst the MODE and UPD links of the

Boundary Scan 120 are linked to the constant activation values equal to 1.

Thus, when the ATPG-mode link of the pin 108 receives an activation signal, the Boundary Scan path 120 and the cells 110 which it comprises are controlled by the signals SI, CK and SE applied to the pin 108 from outside.

In this same case, the signal MODE and the signal UPD which are received by the Boundary Scan chain 120 are the permanent activation signals so that the content of the latches of the input/output cells of the Boundary Scan is substituted for the signals normally tapped off from the pins of these cells during the test according to the invention.

It will be noted that the access path 150 to the memories 140 is permanently linked to the clock input of the pin 108, unlike the Boundary Scan 120 which is tied to the clock signal of the controller 200 or of the pin 108 according to the content of the mode signal applied to the pin 108.

The output of the Boundary Scan chain 120 forms a pin 109 and also carries a link linking this pin 109 to the controller 200, so that the output signal SO from the Boundary Scan 120 is looped back onto the controller 200.

During the test according to the invention, a tester connected to the ATPG-Se, Clock, ATPG-mode and ATPG-Si inputs of the pin 108 activates the concatenated chain comprising the memories 140 in series with the cells 110, and applies a chosen state to the memories 140, imposes a chosen signal on chosen inputs/outputs 100 of the integrated circuit by way of the Boundary Scan chain, and captures signals obtained on inputs/outputs 100 of the integrated circuit by way of the Boundary

Scan chain 120, as well as on the pin 109.

Hence, during the testing of the integrated circuit one uses logic present in the circuit, which logic was used hitherto to access inputs/outputs of the circuit which were inaccessible in particular when this circuit was mounted on a board. The coverage of the testing of a complex integrated logic circuit having numerous inputs/outputs is therefore increased.

A few extra logic gates are added to the circuit so as to couple the Boundary Scan chain 120 to the full-scan ATPG chain, place it in non-transparent mode and couple its clock to the ATPG test clock when the test according to the invention is implemented.

The tester is advantageously furnished with a few channels wired directly to input/output pins 100 of the circuit.

The tester then comprises a module for injecting test signals directly into inputs/outputs linked to these channels and for receiving signals leaving these inputs/outputs 100, and for comparing them with expected signals. The tester then comprises a device for controlling the Boundary Scan chain 120 of the integrated circuit which is coordinated with the direct injection/reception module so as to generate test vectors on sets comprising both inputs/outputs 103 connected directly to the tester and also inputs/outputs 105 connected to the tester via the Boundary Scan chain 120.

In the case of such an association of direct injections and injections by way of the Boundary Scan chain, the test makes it possible to test all the parts of the circuit and turns out to be especially fast, effective, owing in particular to the fact that one uses a tester which has an acceptable number of channels and allows

fast and fuller testing of the circuit.

The injecting of the test vectors by the association of direct injection into the pins and of injection by way of the Boundary Scan chain may even be adopted without resorting to intervention on the memory points.

The concatenating of the ATPG 150 and Boundary Scan 120 chains makes it possible more generally to act on the memories 140 and on the input/output cells 110 through one and the same input 108, with one and the same signal generator.

By virtue of the invention, the number of checking and observation points is increased, and hence the coverage of the test in the vicinity of the inputs/outputs which are left unconnected is improved.

The invention improves the testability in the vicinity of the bidirectional inputs/outputs, even those connected to a channel of the tester, since it provides test access to an intermediate point which according to IEEE standard 1149.1 must form part of the Boundary Scan chain, namely the direction signal.

CLAIMS

1. Process for testing an integrated circuit comprising memory points (140) and a Boundary Scan chain (120), in which one writes and/or reads to and/or from the memory points (140) by way of an access path (150) to the memory points (140) from an outside terminal (108) of the circuit, characterized in that the Boundary Scan chain (120) is activated so as to impose and/or observe logic levels on the inputs/outputs (120) of the integrated circuit.

2. Process according to claim 1, characterized in that the access path (150) to the memory points (140) and the Boundary Scan chain (120) are activated simultaneously.

3. Process according to claim 1 or 2, characterized in that the access path (150) to the memory points (140) and the Boundary Scan chain are activated by way of a line comprising in series the access path (150) to the memory points (140) and the Boundary Scan chain (120).

4. Process according to any one of claims 1 to 3, characterized in that the Boundary Scan chain (120) is activated by way of an activation path (150) linked to the Boundary Scan chain (120) downstream of a TAP controller (200).

5. Process according to claim 4, characterized in that the activation path (150) is linked to the Boundary Scan chain (120) at least by a logic gate (210, 220, 230, 240, 250) able to link, as a function of a control signal (ATPG-mode), the Boundary Scan chain (120) or else to the activation path (150) of the Boundary Scan, or else to the TAP controller (200).

6. Process according to either of claims 4 and 5, characterized in that the activation path (150)

includes at least one channel (ATPG-Si) on which is placed at least one memory point (140), this channel being able to be linked in series with the Boundary Scan chain (120) when the latter is activated.

7. Process according to one of the preceding claims, characterized in that the input channel (Si), clock channel (ck) and configuration channel (Sh) of the Boundary Scan chain (120) are linked to logic gates (210, 220, 230, 240, 250) which are able to link, according to a control signal (ATPG-mode), these channels (Si, ck, Sh) or else to the input channel (Si), clock channel (ck) and configuration channel (Sh) of the TAP controller (200) or else to the input channel (Si), clock channel (ck) and configuration channel (Sh) of the activation path (150).

8. Process according to one of the preceding claims, characterized in that all the memory points (140) are linked in series.

9. Process according to one of the preceding claims, characterized in that at least some of the inputs/outputs (100) of the integrated circuit are connected directly to a tester able to inject chosen signals directly into certain of these inputs/outputs (100), and/or to receive output signals directly from certain of these inputs/outputs (100) and to compare these output signals with expected signals.

10. Process according to one of the preceding claims in combination with claim 9, characterized in that the injection and/or direct measurement tester is coordinated with a device for controlling the Boundary Scan chain (120) so as to generate test vectors on sets comprising both inputs/outputs (103) connected directly to the tester and also inputs/outputs (105) connected to the tester via the Boundary Scan chain (120).

11. Process according to one of the preceding claims, characterized in that the circuit comprises accesses (150) to its set of memory points (140) and in that the test is carried out by controlling the set of memory points (140) so that the function of the integrated circuit is reduced to a combinatorial function.

12. Integrated circuit comprising a Boundary Scan chain (120) and an access path (150) to at least one memory point (140), characterized in that the access path (150) and the Boundary Scan chain (120) are linked in series and in that the circuit comprises means (220, 230, 240, 250) for intervening simultaneously on the memory point or points (140) of the access path (150) and on the cells (110) of the Boundary Scan chain (120).

13. Integrated circuit according to claim 12, characterized in that the means (220, 230, 240, 250) for intervening simultaneously on the memory point or points (140) of the access path (150) and on the cells (110) of the Boundary Scan chain (120) comprise at least one logic gate (220, 230, 240, 250) able to link the Boundary Scan chain (120) or else to the access path (150), or else to a TAP controller (200).

14. Integrated circuit according to claim 12 or 13, characterized in that the input channel (SI), clock channel (CK) and configuration channel (SHIFT) of the Boundary Scan chain (120) are linked to logic gates (220, 230, 240, 250) which are able to link, according to a control signal (MODE), these channels or else to the input channel (SI), clock channel (CK) and configuration channel (SHIFT) of the TAP controller (200), or else to the input channel (ATPG_si), clock channel (ATPG_ck) and configuration channel (ATPG_se) of the access path (150).

15. Integrated circuit according to one of claims 12 to 14, characterized in that all the memory points (140) of the integrated circuit are linked in series.

16. Integrated circuit tester, comprising a first module for imposing and/or reading states of memory points (140) of an integrated circuit, characterized in that it comprises a second module for imposing states and/or reading states of input/output cells (110) by way of the Boundary Scan chain (120) of the circuit simultaneously with the action of the first module.

17. Integrated circuit tester according to claim 16, characterized in that it is contrived so as to simultaneously inject into an integrated circuit, control signals (SI) for the memory points (140) and control signals (SI) for the inputs/outputs (110) of the Boundary Scan (120).

18. Tester according to claim 17, characterized in that it is contrived so as to inject the control signals (51) for the memory points (140) and the control signals (51) for the inputs/outputs (110) of the Boundary Scan (120) onto one and the same channel.

19. Tester according to any one of claims 16 to 18, characterized in that it comprises a series of channels able to be connected directly to inputs/outputs (103) of an integrated circuit, and a module able to inject chosen signals directly into certain of these inputs/outputs (103), and/or to receive output signals from these inputs/outputs (103, 109) so as to compare these output signals with expected signals.

20. Tester according to claim 19, characterized in that it comprises a control device for the Boundary Scan chain (120) of an integrated circuit coordinated with the direct injection/reception module so as to generate test vectors on sets comprising both

inputs/outputs (103) connected directly to the tester and also inputs/outputs (105) connected to the tester via the Boundary Scan chain (120).

21. Tester according to one of claims 16 to 20, characterized in that it is able to control the set of memory points (140) in such a way that the function of the integrated circuit is reduced to a combinatorial function during the test.

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(54) **Title:** METHOD FOR TESTING INTEGRATED CIRCUITS WITH MEMORY ELEMENT ACCESS

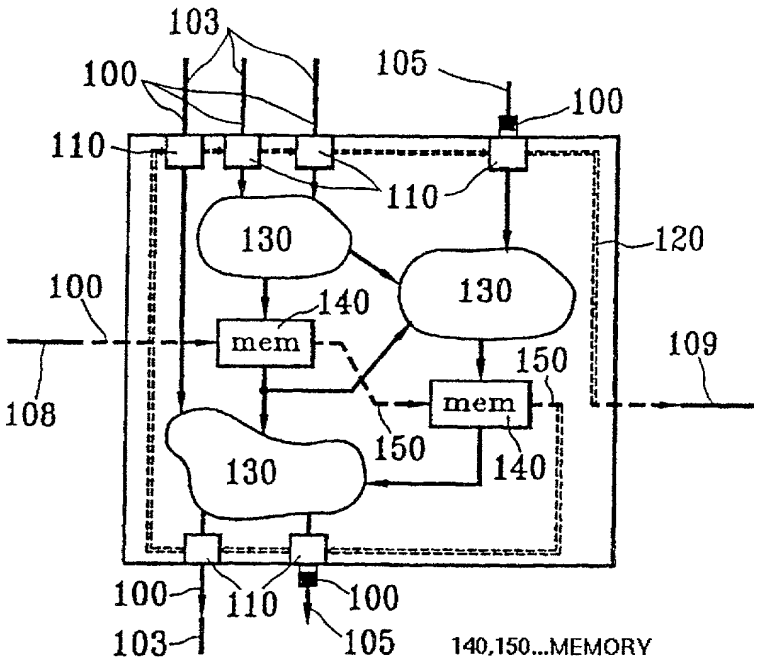
(54) **Titre:** PROCEDE DE TEST DE CIRCUITS INTEGRES AVEC ACCES A DES POINTS DE MEMORISATION DU CIRCUIT

(57) **Abstract**

The invention concerns a method for testing an integrated circuit comprising memory elements (140) and a boundary scan chain (120) wherein on the memory elements (140) can be written and/or read on the memory elements via an access path (150) to the memory elements (140) from a terminal (108) external to the circuit. The invention is characterised in that it consists in activating the boundary scan chain (120) to impose and/or observe logic levels on the integrated circuit inputs/outputs (120).

(57) **Abrégé**

L'invention concerne un procédé pour tester un circuit intégré comprenant des points de mémorisation (140) et une chaîne de Boundary Scan (120), dans lequel on écrit et/ou on lit sur les points de mémorisation (140) par l'intermédiaire d'un chemin d'accès (150) aux points de mémorisation (140) depuis une borne extérieure (108) du circuit, caractérisé en ce que l'on active la chaîne de Boundary Scan (120) pour imposer et/ou observer des niveaux logiques sur les entrées/sorties (120) du circuit intégré.



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	
DOMINIQUE BARTHEL	Art Group:
Application No.:	Examiner:
Filed:	
For: **METHOD FOR TESTING INTEGRATED CIRCUITS WITH MEMORY ELEMENT**	

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF FORMAL DRAWINGS

Sir:

Enclosed herewith for filing in the above-identified U.S. Patent Application are the formal drawings, 3 sheets including 6 Figures. Applicant hereby authorizes any additional extension or petition fees under 37 C.F.R. §1.17 or credit for any overpayment to our Deposit Account No. 02-2666. A copy of the Fee Transmittal sheet is enclosed.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 9/10/01

Eric S. Hyman, Reg. No. 30,139

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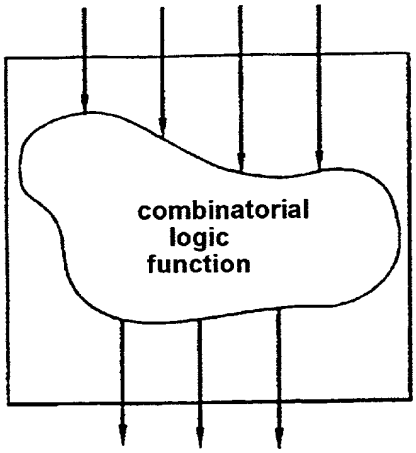

FIG. 1

State of the art

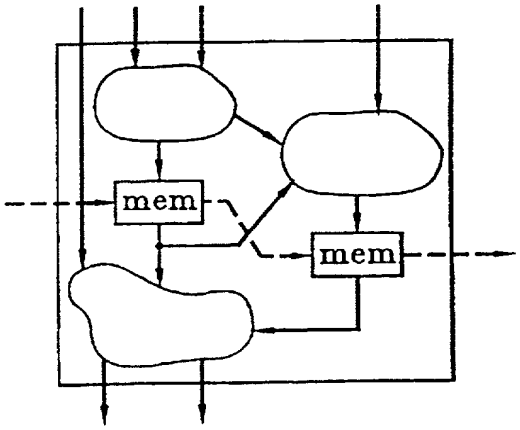

FIG. 2

State of the art

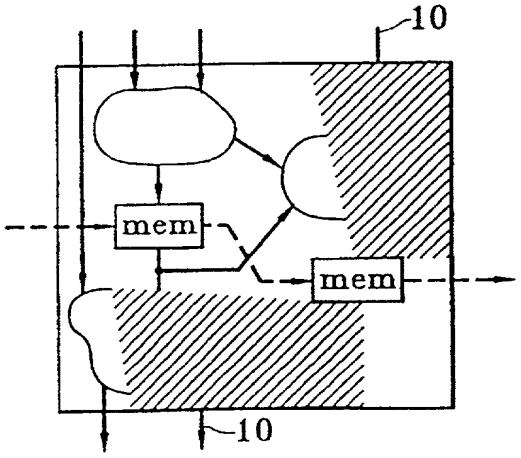

FIG. 3

State of the art

FIG. 4

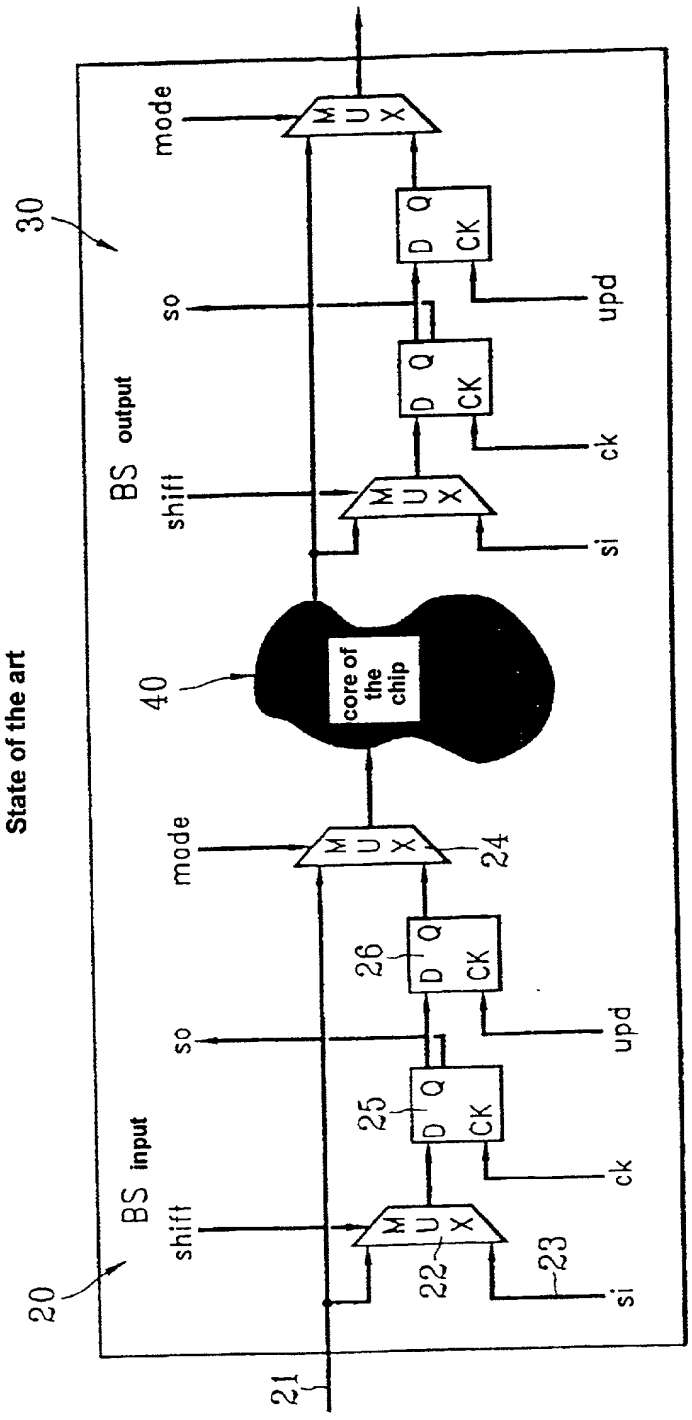
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FIG.5

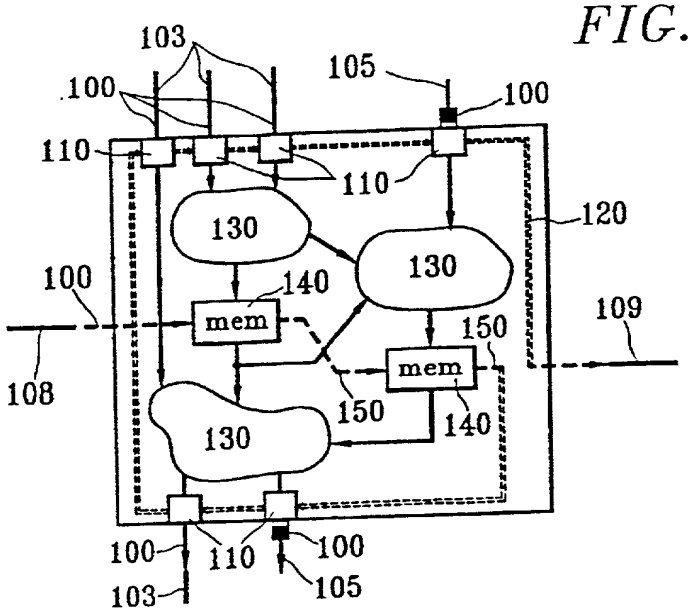
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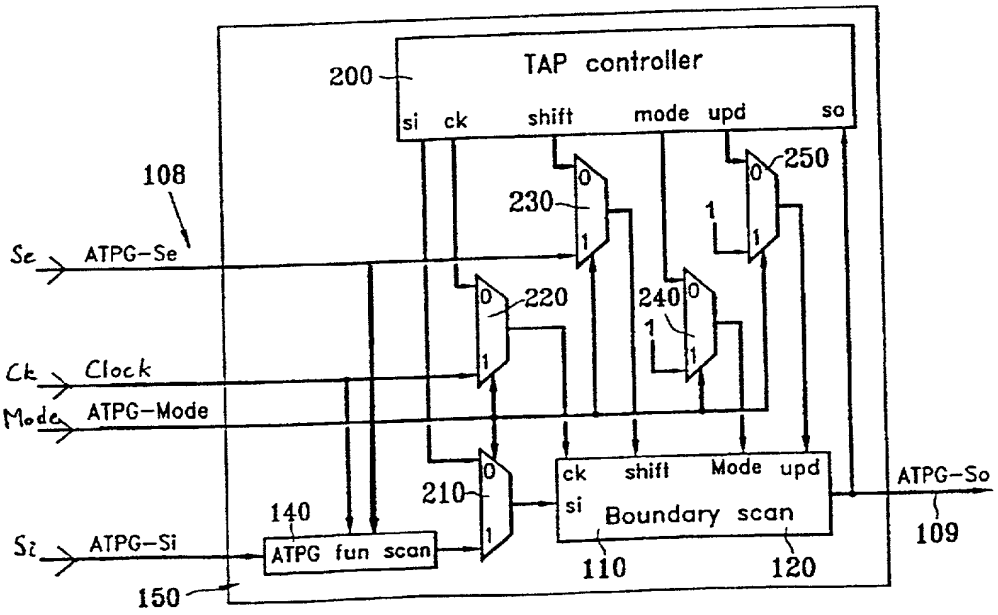
FIG.6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ATPG-So
109
140
Si ATPG-Si
ATPG fun scan
110
120
150

Our Ref.: 13613.1512

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

method for testing integrated circuits with memory element access

the specification of which

____ is attached hereto.
__X__ was filed on March 7, 2000 as
Application Serial No. PCT/FR00/00559
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
99/02823	FRANCE	08.03.1999	X	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PCT/FR00/00559	07.03.2000	pending
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature _____ Date Sept 3rd 2001

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Post Office Address the same as Residence

Full Name of Second/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____